CLAIMS

Please amend the claims as follows:

What is claimed is:

1. (currently amended) A data processing system, comprising:
one or more processing cores; and

a memory controller, coupled to said one or more processing cores, that controls access to a system memory, said memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory, wherein said memory controller ~~includes: means~~, responsive to a memory access request, ~~for~~ speculatively initiates ~~initiating~~ access to the system memory based upon said historical information in said memory speculation mechanism in advance of receipt of a coherency message indicating that said memory access request is to be serviced by reference to said system memory.

2. (original) The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. (original) The data processing system of Claim 1, wherein said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. (original) The data processing system of Claim 1, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

5. (currently amended) The data processing system of Claim 1, wherein said ~~means for speculatively initiating access comprises means for~~ memory controller speculatively initiates ~~initiating~~ access in advance of a combined response for said memory access request.

6. (currently amended) The data processing system of Claim 1, wherein:

said system memory comprises a first system memory;

said memory controller comprises a first memory controller;

said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory;

said memory controller ~~means for speculatively initiating access comprises means for~~ speculatively initiates ~~initiating~~ access to said first system memory based upon historical information recorded by said second memory controller.

7. (original) The data processing system of Claim 1, and further comprising:

a system interconnect coupling said plurality of processing cores; and

one or more cache hierarchies coupled to said plurality of processing cores that cache data from said system memory.

8. (original) The data processing system of Claim 1, and further comprising response logic that provides said combined response for said memory access request.

9. (currently amended) A memory controller for controlling access to a system memory of a data processing system, said memory controller comprising:

a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing ~~to~~ said system memory; and

control logic ~~means~~, responsive to a memory access request, ~~for~~ that speculatively initiates ~~initiating~~ access to the system memory based upon said historical information in said memory speculation mechanism in advance of receipt of a coherency message indicating that said memory access request is to be serviced by reference to said system memory.

10. (original) The memory controller of Claim 9, wherein said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of program threads executing within said data processing system.

11. (original) The memory controller of Claim 9, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

12. (currently amended) The memory controller of Claim 9, wherein said ~~means for speculatively initiating access comprises means for~~ control logic speculatively initiates ~~initiating~~ access in advance of a combined response for said memory access request.

13. (currently amended) The memory controller of Claim 9, wherein said ~~means for speculatively initiating access comprises means for~~ control logic speculatively initiates ~~initiating~~ access to said system memory based upon historical information recorded by another memory controller.

14. (currently amended) A method of operating a memory controller for a system memory of a data processing system, said method comprising:

said memory controller storing in a memory speculation mechanism historical information regarding whether prior memory accesses were serviced by access to the system memory ~~in a memory speculation mechanism~~; and

in response to a memory access request, said memory controller speculatively initiating access to the system memory based upon said historical information in said memory speculation mechanism in advance of receipt of a coherency message indicating that said memory access request is to be serviced by reference to said system memory.

15. (original) The method of Claim 14, wherein said storing comprises storing a respective memory access history for each of a plurality of threads executing within said data processing system.

16. (original) The method of Claim 14, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said storing comprises storing said historical information within said memory speculation table on a per-bank basis.

17. (original) The method of Claim 14, wherein said step of speculatively initiating access comprises

speculatively initiating access in advance of receipt of a combined response for said memory access request.

18. (original) The method of Claim 14, wherein said step of speculatively initiating access comprises speculatively initiating access to said system memory based upon historical information recorded by another memory controller.